UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,808	06/22/2006	**Rohini Krishnan**	NL03 1474 US1	6873

65913 7590 01/27/2009

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
WHITE, DYLAN C	

ART UNIT	PAPER NUMBER
2819	

NOTIFICATION DATE	DELIVERY MODE
01/27/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/583,808	KRISHNAN ET AL.	
	Examiner	Art Unit	
	DYLAN WHITE	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *5 and 6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-4 and 7-14 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

The drawings are objected to because of the following reasons. Figure 5 is objected to because the signal connections of CMN and CMNbar to transistors MP1 & 2 and MN1 & 2 are unclear.

Additionally, Figure 10 is objected to for the following informalities: the gate and body connections of the transistors of Figure 10 are not clear and should be represented more clearly. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after

the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-4, 7-8, and 12-14, are rejected under 35 U.S.C. 102(a) as being anticipated by Chung et al. (U.S. Pat. 7,035,148).

Regarding claim 1, Chung discloses configurable circuit arrangement comprising at least one circuit component at which a load is applied (Fig. 1) that can vary during operation of the circuit arrangement (transistors turned on and off), wherein the configurable circuit arrangement comprises: load determination means (15) for determining a load applied at the at least one configurable circuit component having different fan-in or fan-out depending on a configuration of the circuit arrangement (transistors of Fig. 1); and adjusting means (17) for switching off a buffer (N14-17 and P14-17) connected to the configurable circuit according to the determination of the applied load (at node DQ), wherein switching off the buffer (via transistors P10-13 an

N10-13) adjusts a drive capacity of the at least one circuit (Buffer @ Fig. 1) component to a value less than a maximum drive capacity (any of transistors P10-13 and N10-13 are turned off) while still meeting a delay specification (propagation delay).

Regarding claim 2, Chung discloses wherein the determination means (15) is configured to determine the load based on a configuration information (stored in mode register) loaded to the circuit arrangement (Fig. 1).

Regarding claim 3, Chung discloses wherein the configuration information is stored in a configuration memory (mode registers 15 @ Fig. 1).

Regarding claim 4, Chung discloses wherein the configuration information comprises a configuration bit stream (CL) defining at least one of an input load and an output load of the at least one component (Fig. 1).

Regarding claim 7, Chung discloses wherein the adjusting means (17) is adapted to generate at least one control signal (a0-a3) for simultaneously switching off (non conducting) a section of buffers (P14-17 and N14-17).

Regarding claim 8, Chung discloses wherein the adjusting means (17) is adapted to derive the control signal (a0-a3) from a most significant bit signal of a selection signal obtained from the determination means (mode register 15).

Regarding claim 12, Chung discloses method of controlling power consumption of a configurable circuit arrangement (Fig. 1), the method comprising the steps of: determining a load applied (15) to at least one circuit component having different fan- in or fan-out depending on a configuration of the configurable circuit arrangement (transistors P10-P17 and N10-N17); and switching off (via transistors) a buffer connected to the configurable circuit (Fig. 1) according to the determination of the applied load (at node DQ), wherein switching off the buffer (via transistors) adjusts a drive capacity (number of buffers) of the at least one circuit component (Fig. 1) responsive to the determination step (15) to a value less than a maximum drive capacity (one buffer turned off) while still meeting a delay requirement (propagation delay).

Regarding claim 13, Chung discloses further comprising simultaneously switching off a section of buffers (buffers are simultaneously turned off with update of control code from circuit 17).

Regarding claim 14, Chung discloses further comprising deriving the control signal (a0-a3) from a most significant bit signal of a selection signal (CL).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. Pat. 7,035,148) in view of Ajit (U.S. Pub. 2002/0113628).

Regarding claim 9, Chung discloses that of claim 1 but fails to teach where the adjusting means is configured to vary the threshold voltage of a circuit elements in the arrangement.

Ajit teaches (Fig. 6) changing the transistor threshold voltage by biasing the transistor wells with biasing circuit (401), therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the output buffer disclosed by Schultz with the transistor biasing as taught by Ajit for varying the on/off voltage thresholds of the drive transistors.

Regarding claim 10, the combination discloses where the adjusting means (Ajit; 401 @ Fig. 10) is adapted to change at least one bias voltage (PMOS transistors) in response to the determination means (transistors 1001).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (U.S. Pat. 7,035,148) in view of Schultz (U.S. Pat. 6,445,245).

Regarding claim 11, Chung discloses that of claim 1 but fails to teach where the circuit arrangement is a FPGA.

Schultz discloses an adjustable circuit arrangement wherein the circuit arrangement is a field programmable gate array device (col. 1, lines 13-16), therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the circuit arrangement as disclosed by Chung in the FPGA as taught by Schultz for programmable controlling the output circuit arrangement.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art generally refers to output buffer circuitry and load determination circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DYLAN WHITE whose telephone number is (571)272-1406. The examiner can normally be reached on m-th 7:00- 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dylan White/
Examiner, Art Unit 2819

/Rexford N BARNIE/
Supervisory Patent Examiner, Art Unit 2819